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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,294	12/20/2001	Michael David Church	INT-0001A	8108

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,294	CHURCH, MICHAEL DAVID	
	Examin r	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication app ars on th cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-15 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-15 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

The non-final rejection as set forth in paper No. (11) is withdrawn in response to applicants' amendments.

A new rejection is made as set forth in this Office Action.

Claims (1-3, 6-15, and 17-21) are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3 and 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (U.S. Pub. 2002/0031882) in view of the Applicant's Admitted Prior Art (AAPA).

In re claim 1, **Uchida** discloses a process for making a semiconductor device comprising the steps of (**FIGS. 1-15** and related text):

forming an isolation region **(FIG. 14: 2)** on an epitaxial layer of a semiconductor substrate **(FIG. 14: 60)** to define an active region having a predefined boundary (page 6, paragraph [0080]);

implanting a first dopant into the epitaxial layer within the active region to create a well **(FIG. 14: 16)** of a first type of conductivity (page 6, paragraph [0080]);

implanting the first dopant into the well to create a first region **(FIG. 14: 61)** and a second region **(FIG. 14: 62)** separated from the first region, the first and second regions being implanted across the boundary of the active region and directly spaced apart from

each other across the active region and spaced apart from the center of the active region (page 6, paragraph [0087]);

depositing a polysilicon layer **(FIG. 4: 37)** over the active region (page 6, paragraph [0084]);

doping the polysilicon layer to create a poly semiconductor layer of a second type of conductivity;

patterning the poly semiconductor layer to create a poly gate **(FIG. 14: 29)** over the first and second regions and well (page 6, paragraph [0084]); and

performing an ion implant of the second type conductivity between the LOCOS regions and the poly gate to create first and second lightly doped regions, the first and second lightly doped regions being separated by a channel region beneath the poly gate **(FIG. 14)**;

Uchida fails to explicitly disclose depositing an oxide layer over the poly gate and active region; etching the oxide layer to create side spacers on each side of the poly gate; and implanting a heavy dose of the second type of dopant between the LOCOS regions and the side spacers to create source and drain regions, the source and drain regions being separated by the first and second lightly doped regions and the channel region.

AAPA discloses performing a LOCOS operation on an epitaxial layer of a semiconductor substrate to define an active region having a predefined boundary **(FIG. 3)**; depositing an oxide layer over the poly gate **(FIG. 3: 1)** and active region; etching the oxide layer to create side spacers **(FIG. 3: 7, 17)** on each side of the poly gate; and

implanting a heavy dose of the second type of dopant between the LOCOS regions and the side spacers to create source **(FIG. 3: 3)** and drain **(FIG. 3: 2)** regions, the source and drain regions being separated by the first **(FIG. 3: 5)** and second **(FIG. 3: 15)** lightly doped regions and the channel region (page 8, 2nd pargraph). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Uchida with the AAPA in order to establish a CMOS and BICMOS device structures (page 8, 2nd paragraph).

In re claim 2, **Uchida** discloses wherein the process according to claim 1, further including the step of: implanting the second type of dopant into the semiconductor substrate prior to the step of growing the epitaxial layer (page 4, pargraph [0063] and **FIG. 1**).

In re claim 3, **Uchida** discloses wherein the first type of dopant is a P type dopant and the second type of dopant is an N type of dopant **(FIG. 14)**.

In re claim 6, **Uchida** discloses wherein the first type of dopant is a P type of dopant and the step of performing an implant of the second type of dopant between the LOCOS regions and the poly gate comprises the step of: implanting a light dose of N type dopant with each of the first and second lightly doped regions and positioned to be in contact with the first and second regions (page 6, paragraphs [0079]-[0084] and **FIG. 14**).

In re claim 7, **Uchida** discloses wherein the step of: patterning the poly semiconductor layer to create a poly gate **(FIG. 14: 29)** includes the step of: patterning the poly gate over the first and second regions (page 6, paragraph [0084] and **FIG. 14**).

In re claim 8, **Uchida** discloses wherein the first type of dopant is a P type of dopant and the step of: performing an implant of the second type of dopant between the LOCOS regions and the poly gate comprises the step of: implanting a light dose of N type dopant with each of the first and second lightly doped regions being positioned not to be in contact with the first and second regions (page 6, paragraphs [0079]-[0084] and **FIG. 14**).

In re claim 9, **Uchida** discloses wherein the step of: performing an ion implant of the second type conductivity between the LOCOS regions and the poly gate comprises the step of: implanting a light dose of N type dopant **(FIG. 14)**.

In re claim 10, **Uchida** discloses wherein the step of implanting a heavy dose of a second type of dopant comprises the step of; implanting the heavy dose of N type dopant into the first and second lightly doped regions (page 6, paragraphs [0079]-[0084] and **FIG. 14**).

In re claim 11, **Uchida** fails to explicitly wherein the step of: implanting a heavy dose of the second type of dopant between the LOCOS regions and the side spacers to create source and drain regions, the source and drain regions being separated by the channel region; all included the step of: patterning the active area using a first reticle to create a pattern on the active region (page 8, 2nd paragraph and **FIG. 3**).

AAPA discloses wherein the step of: implanting a heavy dose of the second type of dopant between the LOCOS regions and the side spacers to create source and drain regions, the source and drain regions being separated by the channel region; all included the step of: patterning the active area using a first reticle to create a pattern on the active

region. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Uchida with the AAPA in order to establish a CMOS and BICMOS device structures (page 8, 2nd paragraph).

In re claim 12, **Uchida** discloses wherein the step of: performing an ion implant of the second type conductivity between the LOCOS regions and the poly gate to create first and second lightly doped regions, the first and second lightly doped regions being separated by a channel region beneath the poly gate included the step of: patterning the active area using the first reticle to create a pattern on the active region **(FIG. 14)**.

2. Claims 13-15, and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (U.S. Pub. 2002/0031882) in view of the Applicant's Admitted Prior Art (AAPA).

In re claim 13, **Uchida** discloses a process for making a semiconductor device comprising the steps of (**FIGS. 1-15** and related text):

forming an isolation region **(FIG. 14: 2)** on an epitaxial layer to define an active region;

using the first reticle to create a pattern for implanting a first dopant into the epitaxial layer within the active region to create a well **(FIG. 14: 16)** of a first type of conductivity (page 6, paragraphs [0079]-[0084]);

using a second reticle to create a pattern for implanting with the first type of dopant into the well to create first region **(FIG. 14: 61)** and second regions **(FIG. 14: 62)** across the boundary of the active region and spaced directly apart across the active region from each other and spaced apart from the center of the active region (page 6, paragraph [0087]);

depositing a polysilicon layer **(FIG. 4: 37)** over the active region (page 6, paragraph [0084]);

heavily doping with a second dopant the polysilicon layer to create a poly semiconductor layer of a second type of conductivity;

patterning the poly semiconductor layer to create a poly gate **(FIG.14: 29)** (page 6, paragraph [0084]); and

using a third reticle to create a pattern for lightly doping with a second dopant the active region between the LOCOS regions and the poly gate (page 6, paragraphs [0079]-[0084] and **FIG. 14**);

Uchida fails to explicitly disclose depositing an oxide layer over the poly gate and active region; etching the oxide layer to create side spacers on each side of the poly gate; and using the third reticle to create a pattern for heavily doping with the second dopant the active region between the LOCOS regions and the side spacers.

AAPA discloses performing a LOCOS operation on an epitaxial layer of a semiconductor substrate to define an active region having a predefined boundary **(FIG. 3);** depositing an oxide layer over the poly gate **(FIG. 3: 1)** and active region; etching the oxide layer to create side spacers **(FIG. 3: 7, 17)** on each side of the poly gate; and using the third reticle to create a pattern for heavily doping with the second dopant the active region between the LOCOS regions and the side spacers (page 8, 2nd pargraph). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Uchida with the AAPA in order to establish a CMOS and BICMOS device structures (page 8, 2nd paragraph).

In re claim 14, **Uchida** discloses wherein the process according to claim 1, further including the step of: implanting the second type of dopant into the semiconductor substrate prior to the step of growing the epitaxial layer (page 4, paragraph [0063] and **FIG. 1**).

In re claim 15, **Uchida** discloses wherein the first type of dopant is a P type dopant and the second type of dopant is an N type of dopant (page 6, paragraphs [0079]-[0084] and **FIG. 14**).

In re claim 17, **Uchida** discloses wherein the first type of dopant is a P type of dopant and the step of lightly doping the second type of dopant between the LOCOS regions and the poly gate comprises the step of: implanting a light dose of N type dopant wherein each of the first and second lightly doped regions are in contact with the first and second regions (page 6, paragraphs [0079]-[0084] and **FIG. 14**).

In re claim 18, **Uchida** discloses wherein the step of implanting a heavily doping with the second dopant comprises the step of: implanting the heavy dose of N type dopant into the first and second lightly doped regions (page 6, paragraphs [0079]-[0084] and **FIG. 14**).

In re claim 19, **Uchida** discloses wherein the step of patterning the poly semiconductor layer to create a poly gate **(FIG. 14: 29)** includes the step of: patterning the poly gate over the first and second regions **(FIG. 14)**.

In re claim 20, **Uchida**, wherein the step of using the first reticle to create a pattern for lightly doping with the second dopant the active region beetween the LOCOS

regions and the poly sate comprises the step of: implanting a light dose of N type dopant **(FIG. 14)**.

In re claim 21, **Uchida** discloses wherein the step of: using the first reticle to create a pattem for heavily doping between the LOCOS regions and the poly gate comprises the step of: implanting a heavy dose of N type dopant **(FIG. 14)**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
November 11, 2003

W. DAVID COLEMAN
PRIMARY EXAMINER